In the Claims:

1. (*Currently Amended*) A frequency-domain decision feedback equalizer device for single carrier modulation~~, preferably for use in a broadband communication system, including~~ comprising:

a first section ~~comprising:~~ including

a fast Fourier transforming means for performing a fast Fourier transformation on a first vector of signals inputted into said first section, and outputting a second vector of signals,

a feed forward equalization means for performing a feed forward equalization by multiplying each of the components of said second vector of signals with equalization parameters, and outputting a third vector of signals, and

an inverse fast Fourier transforming means for performing an inverse fast Fourier transformation on said third vector of signals, and outputting a fourth vector of signals; and

a second section ~~comprising:~~ including

a feedback filter means for performing a linear filtering of a signal derived from an output signal of said second section,

an adding means for adding the output signal of said feedback filter means to the output signal of said first section, and

a detector means for receiving the output signal of said adding means and generating said output signal of said second section by extracting samples from the output signal of said adding means.

2. (*Original*) The device according to claim 1, wherein said feed forward equalization means is provided for generating equalization parameters adapted for minimizing the signal-to-noise ratio of the signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section.

3. (*Previously Presented*) The device according to claim 1, wherein said feed forward equalization means is provided for generating equalization parameters by taking into account a fast Fourier transformation estimation of a channel impulse response of the

signal processed in the frequency-domain decision feedback equalizer device, preferably in the output signal of said first section.

4. (*Previously Presented*) The device according to claim 1, wherein said first section further comprises:

a serial to parallel converting means for converting a sequence of signals inputted into said first section to said first vector of signals, and

a parallel to serial converting means for converting said fourth vector of signals to a sequence of output signals of said first section.

5. (*Original*) The device according to claim 4, wherein said serial to parallel converting means is adapted to receive scalar signals.

6. (*Currently Amended*) The device according to claim 4, wherein said signal to parallel converting means is provided to generate said first vector of signals including blocks of a predetermined number ~~(P)~~ of consecutive samples of the signals inputted into said first section.

7. (*Previously Presented*) The device according to claim 4, wherein said parallel to serial converting means and said feedback filter means are provided to output scalar signals.

8. (*Currently Amended*) The device according to claim 6, wherein said parallel to serial converting means is provided to output a scalar signal ~~(Y)~~ which is constituted by consecutive blocks of a predetermined number ~~(M)~~ of samples, each block being built with the predetermined number ~~(M)~~ of samples of each block of said fourth vector of signals.

9. (*Previously Presented*) The device according to claim 1, wherein said detector means is adapted to receive and output discrete time signals.

10. (*Previously Presented*) The device according to claim 1, wherein said detector means is provided to generate said output signal.

11. (*Previously Presented*) The device according to claim 1, wherein said second section further comprises a feedback input generator means for receiving said output signal of said second section and providing an output signal which is built by consecutive blocks, each block including first a pseudo noise sequence and second a predetermined number (M) of samples from said output signal of said section, to said feedback filter means.

12. (*Currently Amended*) The device according to claim 1, further including ~~A~~ a receiver of a communication system using a single carrier modulation, wherein said receiver includes ~~a~~ said first and second sections of the frequency-domain decision feedback equalizer device ~~according to claim 1~~.

Claims 13-16 (*Cancelled*).

17. (*Currently Amended*) The device according to claim 1, further including ~~A~~ a communication system including a transmitter using a single carrier modulation, for transmitting data, comprising a modulating means for organizing the data in blocks wherein each block is separated by a sequence of a predetermined signal and a receiver of a communication system using a single carrier modulation, wherein said receiver includes ~~a~~ said first and second sections of the frequency-domain decision feedback equalizer device ~~according to claim 1~~.

18. (*Previously Presented*) A frequency-domain decision feedback equalizing method for single carrier modulation, preferably for use in a broadband communication system, comprising the steps of:
in a first section:

performing a fast Fourier transformation on a first vector of signals inputted, and as a result providing a second vector of signals,

performing a feed forward equalization by multiplying each of the components of said second vector of signals with equalization parameters, and as a result providing a third vector of signals,

performing an inverse fast Fourier transformation on said third vector of signals, and as a result providing a fourth vector of signals, and

providing an output signal of said first section on the basis of said fourth vector of signals; and

in a second section:

performing a linear feedback filtering of a signal derived from an output signal of said second section, and providing a filtered signal,

adding said filtered signal to said output signal of said first section, and providing an added signal, and

generating said output signal of said second section by extracting samples from said added signal.

19. (*Original*) The method according to claim 18, wherein in said feed forward equalization step equalization parameters are generated adapted for minimizing the signal-to-noise ratio of the signal processed, preferably in the output signal of said first section.

20. (*Previously Presented*) The method according to claim 18, wherein in said feed forward equalization step equalization parameters are generated by taking into account a fast Fourier transformation estimation of a channel impulse response of the signal processed, preferably in the output signal of said first section.

21. (*Previously Presented*) The method according to claim 18, comprising in said first section the further steps of:

serial to parallel converting a sequence of signals inputted into said first section to said first vector of signals, and

parallel to serial converting said fourth vector of signals to a sequence of output signals of said first section.

22. (*Original*) The method according to claim 21, wherein said serial to parallel converting step is provided to process scalar signals.

23. (*Currently Amended*) The method according to claim 21, wherein said signal to parallel converting step is provided to generate said first vector of signals including blocks of a predetermined number ~~(P)~~ of consecutive samples of the signals inputted into said first section.

24. (*Previously Presented*) The method according to claim 21, wherein said parallel to serial converting step and said linear feedback filtering step are provided to output scalar signals.

25. (*Currently Amended*) The method according to claim 23, wherein said parallel to serial converting step is provided to output a scalar signal ~~(Y)~~ which is constituted by consecutive blocks of a predetermined number ~~(M)~~ of samples, each block being built with the predetermined number ~~(M)~~ of samples of each block of said fourth vector of signals.

26. (*Previously Presented*) The method according to claim 18, wherein said extracting step in said second section is adapted to process discrete time signals.

27. (*Previously Presented*) The method according to claim 18, wherein said extracting step in said second section is provided to generate said output signal.

28. (*Currently Amended*) The method according to claim 18, comprising in said second section a feedback input generating step for processing said output signal of said second section and providing an output signal which is built by consecutive blocks, each block including first a pseudo noise sequence and second a predetermined number ~~(M)~~ of samples from said output signal of said section, to said feedback filter means.

Claims 29-32 (*Cancelled*).